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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/749,301	12/31/2003	Andy H. Gan	X-1294 US	9777

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EXAMINER	
LAM, NELSON C	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 02/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/749,301	GAN ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *20 and 21* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12/31/2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/31/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 12/31/2003. Application 10/749,301 has been examined. In the examination of 10/749,301, claims 1-19 are pending.

Election/Restrictions

2. Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-19, drawn to a method of placement of standard cell blocks, classified in class 716, subclass 9.

II. Claims 20-21, drawn to a method of top level placement of programmable logic blocks, classified in class 716, subclass 8.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention I has separate utility such as for selectively scaling an integrated circuit. Invention II has separate utility such as for the improvement of yield. See MPEP § 806.05(d).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim

remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art because of their recognized divergent subject matter, restriction for examination purposes as indicated is proper.

3. During a telephone conversation with Kim Kanzaki (Registration No. 37,652) on 02/16/2006 a provisional election was made with traverse to prosecute the invention of Group I. Affirmation of this election must be made by applicant in replying to this Office action. Claims 20-21 are withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: In Fig. 3, numeral 300 is missing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

6. **Claims 1-19 are rejected under 35 U.S.C. 102(a)** as being anticipated by Wang et al. (US Patent No. 6,594,809).

As per **claim 1**, Wang discloses a method of automatically inserting antenna diodes for an integrated circuit design, comprising:

selecting a block of standard cells defining at least a portion of the integrated circuit design (Abstract; col. 1, line 33-43; col. 2, line 48-52; col. 3, line 53-64);

associating a diode circuit with at least one input port of said block of standard cells to form an augmented block (col. 1, line 33-47; col. 2, line 6-15; where augmented blocks are formed from standard cells); and

implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 2**, Wang discloses the method of claim 1, wherein said implementing step comprises:

laying out components of said augmented block, said components being defined by said block of standard cells (col. 2, line 48-52; col. 5, line 16-21); and

routing conductors for connecting said components (col. 1, line 43-47; col. 2, line 52-53).

As per **claim 3**, Wang discloses the method of claim 2, wherein said diode circuit associated with each said at least one input port comprises a standard cell selected from said cell library (col. 2, line 16-26; col. 2, line 63 to col. 3, line 9).

As per **claim 4**, Wang discloses the method of claim 3, further comprising:

creating placement constraint data for said diode circuit associated with said at least one input port (col. 4, line 11-25).

As per **claim 5**, Wang discloses the method of claim 4, wherein said laying out step comprises placing said diode circuit associated with said at least one input port in accordance with said placement constraint data (col. 4, line 11-25; col. 4, line 39-44).

As per **claim 6**, Wang discloses the method of claim 5, further comprising:

responsive to said implementing step, identifying an antenna violation associated with an offending input port of said at least one input port (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending input port (col. 4, line 11-25; col. 4, line 39-44); and

re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 7**, Wang discloses the method of claim 6, further comprising repeating said identifying step, said associating at least one additional diode step, and said re-implementing step a plurality of times (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 8**, Wang discloses the method of claim 6, wherein said re-implementing step comprises:

replacing at least one filler cell of said augmented block with said at least one additional diode circuit (col. 2, line 63 to col. 3, line 9; Fig. 6, #13; col. 3, line 65-66; Fig. 4, #38; col. 4, line 39-42).

As per **claim 9**, Wang discloses the method of claim 6, wherein said identifying step comprises:

determining a ratio of an area of a conductor associated with said offending input port to an area of a gate of a transistor associated with said offending input port (Fig. 4; col. 4, line 25-32); and

comparing said ratio to a threshold (col. 1, line 56-61; where an antenna rule violation is inherent to a threshold).

As per **claim 10**, Wang discloses the method of claim 1, further comprising:

responsive to said implementing step, identifying an antenna violation associated with an offending input port of said at least one input port (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending input port (col. 4, line 11-25; col. 4, line 39-44); and

re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 11**, Wang discloses the method of claim 1, wherein said at least one input port comprises all input ports of said block (col. 1, line 33-47; col. 2, line 6-15).

As per **claim 12**, Wang discloses an apparatus for automatically inserting antenna diodes for an integrated circuit design, at least a portion of the integrated circuit being defined by a block of standard cells selected from a cell library (col. 1, line 26-32), the apparatus comprising:

means for associating a diode circuit with at least one input port of said block of standard cells to form an augmented block (col. 1, line 33-47; col. 2, line 6-15); and

means for implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 13**, Wang discloses the apparatus of claim 12, further comprising:

means for identifying an antenna violation associated with an offending input port of said at least one input port responsive to said implementing means (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

means for associating at least one additional diode circuit with said offending input port (col. 4, line 11-25; col. 4, line 39-44); and

means for re-implementing said augmented block within said integrated circuit design (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 14**, Wang discloses a method of forming an integrated circuit, comprising:

associating a diode circuit with each of a plurality of primary input ports of an embedded logic circuit defining at least a portion of the integrated circuit, a remaining portion of the integrated circuit defining existing logic circuitry (col. 2, line 63 to col. 3, line 6);

laying out components of said embedded logic circuit (col. 1, line 33-36);

routing conductors connecting said components (col. 1, line 38-49); and

integrating said embedded logic circuit with said existing logic circuitry onto a chip to form the integrated circuit (col. 5, line 16-21).

As per **claim 15**, Wang discloses the method of claim 14, further comprising:

responsive to said integrating step, identifying an antenna violation associated with an offending primary input port of said plurality of primary input ports (col. 1, line 53-61; col. 4, line 8-25; col. 4, line 39-44);

associating at least one additional diode circuit with said offending primary input port (col. 4, line 11-25; col. 4, line 39-44); and

re-integrating said embedded logic circuit with said existing logic circuitry onto said chip (col. 1, line 33-43; col. 2, line 48-53; col. 5, line 16-21).

As per **claim 16**, Wang discloses the method of claim 15, wherein said components of said embedded logic circuit, said diode circuit associated with each of a plurality of primary input ports, and said additional diode circuit are composed of standard cells selected from a cell library (col. 2, line 16-26; col. 2, line 63 to col. 3, line 9).

As per **claim 17**, Wang discloses the method of claim 16, further comprising replacing at least one filler cell of said embedded logic circuit with said at least one additional diode circuit (col. 2, line 63 to col. 3, line 9; Fig. 6, #13; col. 3, line 65-66; Fig. 4, #38; col. 4, line 39-42).

As per **claim 18**, Wang discloses the method of claim 14, wherein said integrated circuit is a programmable logic device and at least a portion of said existing logic circuitry comprises programmable logic blocks (col. 1, line 16-20; col. 5, line 16-21).

As per **claim 19**, Wang discloses the method of claim 18, wherein said embedded logic circuit is a processor (col. 1, line 16-20; col. 5, line 16-21).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday at 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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SUPERVISORY PATENT EXAMINER